IN THE CLAIMS

Please amend the claims as follows:

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9. (Previously Presented): A clock distribution circuit comprising:

a clock source to generate a clock signal;

a clock divider to divide the clock signal and produce a divided clock signal, and including a flip-flop that introduces a first propagation delay to the divided clock signal; and

a delay matching circuit to distribute the clock signal, and to introduce a second propagation delay to the clock signal, the second propagation delay substantially matching the first propagation delay introduced in the divided clock signal by the flip-flop, wherein the delay matching circuit includes:

a multiplexer having a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to the clock source to selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, wherein the transmission gates are configured to correspond substantially to a slave transmission gate in the flip-flop;

a PMOS transistor having a drain coupled to the first input, a gate coupled to ground, and a source coupled to a supply voltage, wherein the PMOS transistor is configured to correspond substantially to a PMOS transistor in a master output driver of the flip-flop; and

an NMOS transistor having a drain coupled to the second input, a gate coupled to the supply voltage, and a source coupled to ground, wherein the NMOS transistor is configured to correspond substantially to an NMOS transistor in the master output driver of the flip-flop.

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10. (Original): The circuit of claim 9, wherein the PMOS transistor is configured to correspond substantially in size to the PMOS transistor in the master output driver of the flip-flop, and the NMOS transistor is configured to correspond substantially in size to the NMOS transistor in the master output driver of the flip-flop.

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16. (Currently Amended): A delay matching circuit comprising:

a multiplexer coupled to a clock source;

transmission gates within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop;

inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop;

an output coupled to the multiplexer to substantially mimic characteristics of an output driver in the flip flop; and

a PMOS transistor having a drain coupled to a first one of the inputs, a gate coupled to ground, and a source coupled to a supply voltage, wherein the PMOS transistor is configured to correspond substantially to a PMOS transistor in a master output driver of the flip-flop; and

an NMOS transistor having a drain coupled to a second one of the inputs, gate coupled to the supply voltage, and a source coupled to ground, wherein the NMOS transistor is configured to correspond substantially to an NMOS transistor in the master output driver of the flip-flop.

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20. (Previously Presented): A delay matching circuit comprising:

a multiplexer having a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to a clock source to

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selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, wherein the transmission gates are configured to correspond substantially to a slave transmission gate in a flip-flop;

a PMOS transistor having a drain coupled to the first input, a gate coupled to ground, and a source coupled to a supply voltage, wherein the PMOS transistor is configured to correspond substantially to a PMOS transistor in a master output driver of the flip-flop;

an NMOS transistor having a drain coupled to the second input, a gate coupled to the supply voltage, and a source coupled to ground, wherein the NMOS transistor is configured to correspond substantially to an NMOS transistor in the master output driver of the flip-flop; and

an inverter coupled to the output of the multiplexer, wherein the inverter is configured to correspond substantially to an output driver in the flip flop.

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25. (Previously Presented): A circuit comprising:

a signal source to generate a signal;

a signal distribution circuit to modify the signal and distribute a modified signal, and including a flip-flop that introduces a first propagation delay in the modified signal; and

a delay matching circuit to distribute the signal, and introduce a second propagation delay to the signal, the second propagation delay substantially matching the first propagation delay introduced in the modified signal by the flip-flop,

wherein the delay matching circuit includes a multiplexer having a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to the signal source to selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, wherein the transmission gates are configured to correspond substantially to a slave transmission gate in the flip-flop, wherein the delay matching circuit further includes:

a PMOS transistor having a drain coupled to the first input, a gate coupled to ground, and a source coupled to a supply voltage, wherein the PMOS transistor is configured to correspond substantially to a PMOS transistor in a master output driver of the flip-flop; and

an NMOS transistor having a drain coupled to the second input, a gate coupled to the supply voltage, and a source coupled to ground, wherein the NMOS transistor is configured to correspond substantially to an NMOS transistor in the master output driver of the flip-flop.

26. (Original): The circuit of claim 25, wherein the PMOS transistor is configured to correspond substantially in size to the PMOS transistor in the master output driver of the flip-flop, and the NMOS transistor to configured to correspond substantially in size to the NMOS transistor in the master output driver of the flip-flop.

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32. (Previously Presented): A method comprising:

dividing a clock signal with a flip-flop to produce a divided clock signal, and to introduce a propagation delay to the divided clock signal; and

introducing a second propagation delay to the clock signal with a delay matching circuit, the second propagation delay substantially matching the first propagation delay introduced in the divided clock signal by the flip-flop, wherein the delay matching circuit substantially mimics delay characteristics of the flip-flop,

wherein the delay matching circuit includes a multiplexer having a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to the clock source to selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, and wherein the transmission gates are configured to correspond substantially to slave transmission gates in the flip-flop, wherein the delay matching circuit includes:

a PMOS transistor having a drain coupled to the first input, a gate coupled to ground, and a source coupled to a supply voltage, wherein the PMOS transistor is configured to correspond substantially to a PMOS transistor in a master output driver of the flip-flop; and

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an NMOS transistor having a drain coupled to the second input, a gate coupled to the supply voltage, and a source coupled to ground, wherein the NMOS transistor is configured to correspond substantially to an NMOS transistor in the master output driver of the flip-flop.

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